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TITLE: SERIAL DATA MAPPING APPARATUS FOR SYNCHRONOUS DIGITAL HIERARCHY SYSTEM

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SERIAL DATA MAPPING APPARATUS FOR SYNCHRONOUS DIGITAL HIERARCHY SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates to a mapping apparatus, and, more particularly, to an apparatus for mapping DS serial data to VC parallel data.

2. Background of the Related Art

[2] Generally, a synchronous digital hierarchy (SDH) system performs a mapping operation for an asynchronous signal according to an ITU-T recommendation. That is, the SDH system performs mapping and pointer processing of the asynchronous signal in a virtual container. After the mapping and processing are complete, the SDH system multiplexes the signal to form a synchronous transmission module STM-1 signal. Therefore, in order to transmit a certain asynchronous signal through the SDH system, a series of processes for changing the corresponding asynchronous signal to an STM-n signal should be performed.

[3] Figure 1 is a block diagram showing a general SDH system. A plurality of VC11/12 virtual containers (11A-11C) map the asynchronous signals DS-1 and DS-1E as VC11/12 signals, in a manner determined by control signals J1, mj1, and Plden of an STM-1 counter 15. In addition, a tributary unit group (TUG) circuit (not shown) attaches a path overhead (POH) and a pointer on the VC11/12 signal, which is mapped in the VC11/12 virtual containers 11A-11C, and arranges them as Tributary Unit (TU) signals. After that, the TUG

circuit multiplexes the arranged TU signals by a ratio of 1:7 and outputs the TUG signal.

[4] A VC3/4 mapping unit 12A receives the multiplexed TUG signal and the asynchronous signals DS-3, DS3E, and DS4 and maps them as VC3/4 signals, according to address signals J1 and mj1 of the STM-1 counter. VC3/4 mapping units 12B and 12C receive the multiplexed TUG signals and the asynchronous signals DS-3 and DS3E and map them as the VC3 signal, according to address signals J1 and mj1 of the STM-1 counter 15. Address signals J1 and mj1 designate the positions where the asynchronous signals are mapped.

[5] Therefore, an AUG3/4 pointer generating unit 13 pointer processes the VC3 signal and the VC4 signal and outputs the administration unit signals AU3 and AU4. An AU signal mapper 14 multiplexes the AU3 and AU4 signals, output from the AUG3/4 pointer generating unit 13, to form an STM-1 signal.

[6] As described above, in the series of processes for receiving the asynchronous signals and generating the STM-1 signal, the mapping operations of the VC11/12 virtual container 11A-11C are performed by a buffer disposed as a channel unit, and by a controlling signal inputted into the buffer, as shown in Figure 2.

[7] Figure 2 is a detailed block diagram showing respective VC11/12 virtual containers 11A-11C. The VC11/12 virtual containers 11A-11C comprise: an elastic buffer 21 for temporarily storing the asynchronous signals DS-1 and DS-1E, that is, serial data; a serial/parallel changing unit 22 for changing the serial asynchronous data Sd read from the elastic buffer 21 into parallel asynchronous data Pd; a VC1 mapper 23 for multiplexing the

parallel asynchronous signal Pd changed in the serial/parallel changing unit 22, and for outputting VC1/VC12 signals; a VC1 framer 24 for controlling the multiplexing operation of the VC1 mapper 23; a write pointer generating unit 25 for generating a write address (WA) of the elastic buffer 21; and a read pointer generating unit 26 for generating a read address (RA) of the elastic buffer 21. The ien and Spen are enable signals of the read pointer generating unit 26 and the serial/parallel changing unit 22, respectively.

[8] When a 1.544 MHz DS-1 signal or a 2.048 MHz DS-1E signal is inputted, the elastic buffer 21 disposed in the respective channel stores the inputted asynchronous DS-1 or DS-1E signal on a position, which the write address WA of the write pointer generating unit 25 sets.

[9] The VC1 framer 24 is inputted the address signal J1 and mj1 from the STM-1 counter 15 and outputs the enable signals ien and Spen to the read pointer generating unit 26 and to the serial/parallel changing unit 22. Also, the VC1 framer 24 generates mapping control signals V5t, J2t, N2t, and K4t indicating the positions on which the new serial asynchronous signals are mapped. Additionally, the VC1 framer 24 generates the control signals J2dt (8:0), Psr, and Nsr indicating the positions on which the data/null data are inserted periodically.

[10] The read pointer generating unit 26 outputs the read address RA according to the enable signal ien outputted from the VC1 framer 24, and the elastic buffer 21 outputs serial asynchronous signal Sd to the serial/parallel changing unit 22, according to the read address RA. The VC1 framer 24 monitors the difference between the write address WA and the read address

RA, and controls the data reading speed by controlling the clock number of the enable signal ien.

[11] Therefore, the serial asynchronous signal Sd read in the elastic buffer 21 is changed into parallel data Pd in the serial/parallel changing unit 22. The VC1 mapper 23 multiplexes the parallel asynchronous signal Pd, changed in the serial/parallel changing unit 22, and outputs VC11/VC12 signal according to the mapping controlling signals V5t, J2t, K4t, J2dt (8:0), Psr and Nsr outputted from the VC1 framer 24.

[12] However, the background art SDH system processes the asynchronous signal by including the elastic buffer 21, the write pointer generating unit 15, the read pointer generating unit, and the serial/parallel changing unit 22 in a respective channel. Therefore, as shown in Figure 1, if the background art SDH system processes 84 channels of DS-1 signals, it needs 84 write pointer generating units, read pointer generating units, and serial/parallel changing units, respectively. In addition, in the background art SDH system, the number of gates needed to implement the respective channels are increased in the case of a multiple channel embodiment, whereby the system structure is complex.

[13] Also, the background art SDH system performs write and read operations of the elastic buffer using the clock signal of the asynchronous signal and the system clock signal, respectively, which are not synchronized with each other. The lack of synchronization creates a system jitter.

SUMMARY OF THE INVENTION

[14] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[15] Therefore, an object of the present invention is to provide a data mapping apparatus for synchronous digital hierarchy system by which mapping operations of multiple channels are performed effectively using the least number of gates.

[16] To achieve the object of the present invention, as embodied and broadly described herein, there is provided a serial data mapping apparatus for an SDH system comprising: a STM-1 address generating unit for generating a mapping address; a VC mapping unit for mapping DS asynchronous signal into VC signal as a byte unit according to the mapping address; and an STM-1 formatting unit for generating an STM-1 signal by pointer processing and multiplexing a virtual container of the mapped VC signal.

[17] The respective VC mapping unit comprises: a plurality of elastic buffers for writing the DS asynchronous signal as a bit unit, and reading the signal as a byte unit; a write pointer generating unit for generating write addresses of respective elastic buffers; a read pointer controlling unit for generating read addresses of respective elastic buffers; a VC1 mapper for multiplexing the parallel asynchronous data of the byte unit read in the respective elastic buffer as VC signals according to a format controlling signal; a VC1 framer identifying mapping position of the asynchronous signal according to a format address signal outputted from the STM-1 address generating unit, and controlling the elastic buffer, the read pointer generating unit, and the VC1 mapper according to the identified mapping position.

[18] The objects of the present invention can be achieved in whole or in part by a serial data mapping apparatus, including a plurality of elastic buffers that each receive serial asynchronous data, store the received asynchronous data, and simultaneously output a number of parallel data bits of the asynchronous data in a multiple bit unit; and a virtual container mapping unit that receives the multiple bit unit from the elastic buffer and maps the multiple bit unit to a virtual container signal.

[19] The objects of the present invention can be further achieved in whole or in part by a method of mapping serial data mapping, including receiving each of a plurality of serial asynchronous data signals into a plurality of elastic buffers, respectively; multiplexing multiple bit data units simultaneously read from the plurality of elastic buffers into a virtual container signal; and generating an STM-1 signal from the virtual container signal.

[20] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[21] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[22] Figure 1 illustrates a general synchronous digital hierarchy system;

[23] Figure 2 illustrates a detailed block diagram showing the VC11/12 virtual container in Figure 1;

[24] Figure 3 illustrates a serial data mapping apparatus for a synchronous digital hierarchy system according to the present invention; and

[25] Figure 4 illustrates a detailed block diagram showing the VC mapping unit in Figure 3.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[26] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[27] Figure 3 is a block diagram showing a serial data mapping apparatus for a synchronous digital hierarchy system according to a preferred embodiment of the present invention. As shown therein, the serial data mapping apparatus comprises an STM-1 address generating unit 41 generating a mapping address stm1 indicating a mapping position of new data; a VC mapping unit 43 for mapping the DS asynchronous signals DS-1, DS-1E, DS3E, and DS4E as VC signals VC11, VC12, VC3, and VC4 according to the mapping address stm1; and an STM-1 formatter 42 for pointer processing and multiplexing a virtual container of the VC signal outputted from the VC mapping unit 42, whereby an STM-1 signal is generated.

[28] As shown in Figure 4, the VC mapping unit 43 comprises a plurality of elastic buffers 31 for storing the asynchronous DS-1 signal of 84 channels and DS-1E signals of 63

channels; a write pointer generating unit 32 generating write addresses WA of the elastic buffers 31; a read pointer controlling unit 33 generating a read address RA of the elastic buffer 31; a VC1 mapper 34 multiplexing parallel asynchronous data Pd of the byte unit, read in the elastic buffers 31, as VC signals VC11/VC12 according to a format controlling signal; and a VC1 framer 35 for identifying the mapping position of asynchronous signals according to the format address stm1 of the STM-1 address generating unit 41, and controlling operations of the elastic buffers 31, the read pointer controlling unit 33, and the VC1 mapper 34 according to the identified mapping position.

[29] When an stm1 address of a format, which will be mapped, is outputted from the STM-1 address generating unit 41, the mapping position of the asynchronous signal is decided by the format address stm1. Once the mapping position is decided, the VC mapping unit 43 performs mapping operations for all asynchronous signals, that is, for 84 channels of DS-1 signals and 63 channels of DS-1E signals collectively. The DS signals are mapped as VC signals VC11, VC12, VC3 and VC4. Therefore, the STM-1 formatter 42 pointer processes and multiplexes the signals VC11, VC12, VC3 and VC4 which are mapped in the VC mapping unit 43 and outputs STM-1 signal.

[30] Hereinafter, the operation of the VC mapping unit 43 will be described in more detail. The inputted 84 channels of DS-1 signals and the 63 channels of DS-1E signals are stored in the plurality of elastic buffers 31 respectively, according to the write address WA outputted from the write pointer generating unit 32. Then, the inputted serial asynchronous signals are synchronized and stored using a system clock signal of 19.44 Mhz, to restrain

generation of a jitter. Therefore, the asynchronous signals are written and read in the elastic buffers 31 according to the system clock signal, whereby the jitter generation generated by a difference between the read and write clock signals is reduced.

[31] The VC1 framer 35 chooses one buffer among the 84 elastic buffers 31 and generates sts1/group/channel SONET addresses for controlling the read pointer controlling unit 33. Consequently, a certain elastic buffer 31 is chosen for generating the sts1/group/channel addresses and the read pointer controlling unit 33 generates a read address RA and outputs it to the chosen elastic buffer 31.

[32] That is, the read pointer controlling unit 33 does not read the data as a bit unit from the elastic buffer 31, instead it reads the data a byte unit (8 bit). Accordingly, the read pointer controlling unit 33 controls a read pointer generating unit (not shown) and outputs a read address, that is, a start bit of 8 bit data to the elastic buffer 31. Then the elastic buffer 31 outputs a parallel asynchronous signal of 8 bits according to the start bit. At that time, the read pointer controlling unit 33 increases the read address RA by +8 in order to read the next 8 bits of data.

[33] However, in the asynchronous signals stored in the elastic buffers 31, a STUFF bit, that is, Null data is included as well as the data signal. Therefore the read pointer controlling unit 35 judges whether the read address RA is increased by +8, +6, or by +4 according to controlling signals Ctrlen and ien outputted from the VC1 framer 34 and, after that, generates a start bit of the read address RA of the asynchronous signal which will be read next time.

[34] Also, the read pointer controlling unit 33 controls the operation speed of the read

pointer generating unit according to controlling signals Psr and Nsr outputted from the VC1 framer 35. That is, the read pointer controlling unit 33 increases by +1 or decreases by –1 the operation speed of the read pointer generating unit according to the controlling signals Psr and Nsr, which are designating the difference between the read address RA and the write address WA.

[35] The VC1 framer 35 generates mapping control signals V5t, J2t, N2t, and K4t designating the mapping position of the serial asynchronous signal according to the STM1 format address outputted from the STM-1 address generating unit 41. VC1 framer 35 also controls signals J2dt (8:0), Psr and Nsr indicating an insertion position of the asynchronous data and the Null data periodically. Also, the VC1 framer 35 generates controlling signals Ctrlen and ien for increasing the read address of the elastic buffer 31 by +8, +6, or +4. Therefore, the VC1 mapper 34 multiplexes the parallel asynchronous signal Pd of 8 bits read in the elastic buffer 31, according to the mapping controlling signals V5t, J2t, N2t, K4t, J2dt (8:0), Psr, and Nsr and the controlling signals Ctrlen and ien outputted from the VC1 framer 35, and generates the VC11/VC12 signal.

[36] The asynchronous data stored in the elastic buffers are read and processed as a byte unit and, therefore, there is no need to include the serial/parallel changing unit as in the background art. Also, in order to perform the write operation of the plurality of elastic buffers, there is provided one write pointer generating unit and one read pointer controlling unit, whereby the system can be constructed in simple way.

[37] In addition, the write and the read operations of the elastic buffers are performed

by synchronizing with the system clock signal, whereby the jitter, which may be generated by the different frequency of the clock signal in the background art, can be reduced effectively.

[38] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.